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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,146	03/19/2004	Yu Pen Tsai	4459-141	6402

7590 03/08/2006

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EXAMINER	
ARORA, AJAY	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,146	TSAI ET AL.	
	Examiner	Art Unit	
	Ajay K. Arora	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 3/19/04 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 08/29/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Peterson (US 2003/0157762), hereinafter Peterson.

Regarding claim 1, Figures 1 and 2 of Peterson disclose a chip scale package comprising: a plurality of terminals (114) for making external electrical connections (page 3, para [0031], last sentence); a chip (110) having a plurality of bonding pads on an active surface thereof (page 3, para [0031], 2nd last sentence), the bonding pads electrically connected to the terminals (page 3, para [0031], last sentence), wherein a backside surface of the chip is exposed from a surface of the chip scale package and an ink mark formed on the backside surface (page 3, para [0032], 1st sentence).

Note that Peterson discloses packaged devices (page 3, para [0030], 1st sentence), which includes chip scale packages (page 1, para [0004]). Further note that Peterson cites that the mark is formed with a marking medium 10 comprising underlying contrast

film 132 and the outer contrast film 134 marking medium (page 5, para [0042], 2nd sentence), wherein 132 and 134 can be inks (page 4, para [0035], last sentence).

Regarding Claim 2, Peterson discloses a method for marking a chip scale packages, the method comprising the following steps: providing a wafer (100) having a plurality of dice (110) formed thereon, wherein the dice have been packaged into a plurality of semi-finished chip scale packages, wherein the semi-finished chip scale packages comprises a plurality of terminals (114) for making external electrical connections (page 3, para [0031], last sentence), each die has a plurality of bonding pads on an active surface thereof, the bonding pads are electrically connected to the terminals (page 3, para [0031], last sentence), and a backside surface of each die is exposed from a surface of the semi-finished chip scale packages; positioning the semi-finished chip scale packages formed on the wafer; printing ink marks on the exposed backside surface of the dice (page 3, para [0032], 1st sentence); curing the ink marks on the dice (page 4, para [0038], 2nd sentence); and dicing the wafer (page 3, [0033], last sentence) to obtain a plurality of chip scale packages wherein each package is separated from other packages.

Regarding Claim 3, Peterson teaches the method further comprising a step of removing defective ink marks after the printing step and before the curing step (page 4, para [0038], 4th sentence).

Regarding Claim 7, Figure 1 and 2 of Peterson teach a semiconductor wafer (100) comprising a plurality of dice (110) wherein each of dice has a plurality of bonding pads (array 114) on an active surface thereof and an ink mark (132 and 134) on a backside surface thereof.

Regarding Claim 8, Figure 1 and 2 of Peterson teach a semiconductor die (110) comprising a plurality of bonding pads (array 114) on an active surface thereof and an ink mark (132 and 134) on a backside surface thereof.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson as applied to claims 1-3 and 7-8 above, and further in view of Schramm (US 2004/0060910), hereinafter Schramm.

Regarding Claim 4 and 6, Peterson teaches the method as claimed in claim 2, wherein the positioning step is performed by a positioning device (page 1, para [0005], 2nd last

sentence) and the printing step is performed by a printing device (page 6, para [0049], 3rd line). However, Peterson does not teach that "the positioning device and the printing device are positioned on two opposing sides of the wafer, and the printing step is performed by coaxially aligning the printing device with the positioning device". Figure 2c of Schramm teaches a system for marking semiconductor wafers wherein the positioning device (142) and the printing device (147) are positioned on two opposing sides of the wafer (143), and the printing step is performed by coaxially aligning (along 149) the printing device with the positioning device. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Peterson with the teachings of Schramm so that the positioning device and the printing device are positioned on two opposing sides of the wafer, and the printing step is performed by coaxially aligning the printing device with the positioning device. The ordinary artisan would have been motivated to modify Peterson for at least the purpose of improving positional accuracy.

Regarding Claim 5, Figure 2 of Peterson (page 3, para [0033], last line) teaches the wafer has a plurality of dicing streets (117) between the semi-finished chip scale packages. However, Peterson fails to teach that "the position step is performed by finding the dicing street with a charge coupled device (CCD)". Schramm discloses a system for processing semiconductor wafers wherein the position step is performed by finding the dicing street (page 5, para [0078], 10th sentence) with a charge coupled device (page 5, para [0076], 1st line). It would have been obvious to one of ordinary

skills in the art at the time of the invention to modify the invention of Peterson with the teachings of Schramm so that the position step is performed by finding the dicing street with a charge coupled device (CCD). The ordinary artisan would have been motivated to modify Peterson for at least the purpose of utilizing widely available off-the-shelf positioning equipment.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ajay K. Arora whose telephone number is (571) 272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800